A 3–5 GHz Current-Reuse g_m-Boosted CG LNA for Ultrawideband in 130 nm CMOS

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***Abstract*—This paper presents a low-power CMOS transconductance "g_m" boosted common gate (CG) ultrawideband (UWB) low noise amplifier (LNA) architecture, operating in the 3–5 GHz range, employing current-reuse technique. This proposed UWB CG LNA utilizes a common source (CS) amplifier as the g_m-boosting stage which shares the bias current with the CG amplifying stage. A detailed mathematical analysis of the LNA is carried out and the different design tradeoffs are analyzed. The LNA circuit was designed and fabricated using the 130-nm IBM CMOS process and it achieved input return loss (S_{11}) and output return loss (S_{22}) variations of respectively -8.4 to -40 dB and -14 to -15 dB within the pass-band. The LNA exhibits almost flat forward power gain (S_{21}) of 13 dB and a reverse isolation (S_{12}) variation of -55 dB to -40 dB, along with a noise figure (NF) ranging between 3.5 and 4.5 dB. The complete circuit (with output buffer) draws only 3.4 mW from a 1 V supply voltage.**

***Index Terms*—CMOS noise optimization, common gate amplifier, current-reuse, g_m-boosted low noise amplifier (LNA), LNA, ultrawideband (UWB).**

I. Introduction

THE overwhelming technological advancements have reduced the CMOS device dimensions considerably. Hence, for system-on-chip (SOC) designs, the ability to integrate digital, analog and RF building blocks with low power consumption is an acute necessity. Also, scaling to nanometric dimensions have resulted in CMOS devices achieving transit frequencies (f_T) comparable to those of bipolar junction transistors (BJTs) [1]–[3]. Since the Federal Communications Commission (FCC) defined the frequency spectral mask for the ultra-wideband (UWB) radios and authorized this technology for commercial use in 2002 [4], [5], UWB has been the emerging broadband wireless technology that promises connectivity within the 3.1–10.6 GHz band. It has been of great significance for the academic and industrial communities to investigate better techniques to realize UWB transceiver using the "continually shrinking" CMOS technologies (e.g., [6]–[15]). Various methods of pulse shaping and pulse modulation can be adopted to utilize the vast UWB spectrum. The WiMedia Alliance proposes a physical layer specification which divides the UWB spectrum into 14 528 MHz wide sub-bands [16]. The sub-bands are further combined into five band-groups as shown in Fig. 1 [42] and [43].

Similar to a narrowband RF system, LNA plays an imperative role in the CMOS UWB radio receiver front-end. In published literature, several techniques have been reported to impart high performance in the design of the UWB LNA. Based on the input matching characteristics and noise performance, the published CMOS UWB LNA architectures can be divided into two major groups, the common source (CS), and the common gate (CG) LNA [11], [17]. General topology of these architectures is shown in Fig. 2. The noise factor of the CS LNA with inductive source degeneration is linear with the operating angular frequency and can be large in the gigahertz range as its output gate current noise increases with the increase in ω. This architecture is inherently narrowband and achieving wideband input match to the signal source in the presence of the parasitic capacitances (e.g., bond pad, package, and board traces) is quite difficult [19], [20]. In this case, advanced design techniques are required to provide wideband input match to meet UWB matching requirements [13] and [14]. On the other hand, the CG LNA noise factor, although slightly higher as compared to its counter part, is almost independent of ω and remains nearly constant irrespective of the bandwidth and the frequency of operation. Also, achieving wideband input match and absorbing parasitic capacitances is relatively simple and is less effected by process variations in the case of the CG topology. The CG UWB LNA shown in Fig. 2(b), has a parallel resonant resistor inductor capacitor (RLC)-network with the quality factor, $Q = \omega C_{gs} R_s/2$ ignoring other parasitics and the body effect. As the Q is proportional to the gate-to-source capacitance C_{gs}, it would decrease with shrinking technology and hence, the bandwidth would demonstrate a broadband behavior. Therefore, the CG LNA can easily be adopted for broadband impedance matching without many extra components [11]. Although, the NF of the CG LNA $(\approx 1 + [\gamma/\alpha])$ [35] depends on the device size and process parameters, it remains almost constant with ω. Also, the NF of the CG LNA has a strong coupling with the bias point, or, in other words, the $1/g_m$ input matching resistance looking into the source. Reduction in the output noise floor of the CG LNA is achieved by using the g_m-boosting technique that decouples the input matching and the NF of the CG LNA [15], [17], [18].

Current reuse technique has been used in many recent LNA topologies [21]–[31] to reduce power consumption in mobile devices. This paper reports a low-power CG UWB LNA architecture which implements a novel "current-reused g_m-boosting" technique. The topology also includes a front-end passive LC-band-pass filter for broadband input matching with sharp out-of-band roll-off. The circuit operates in the UWB

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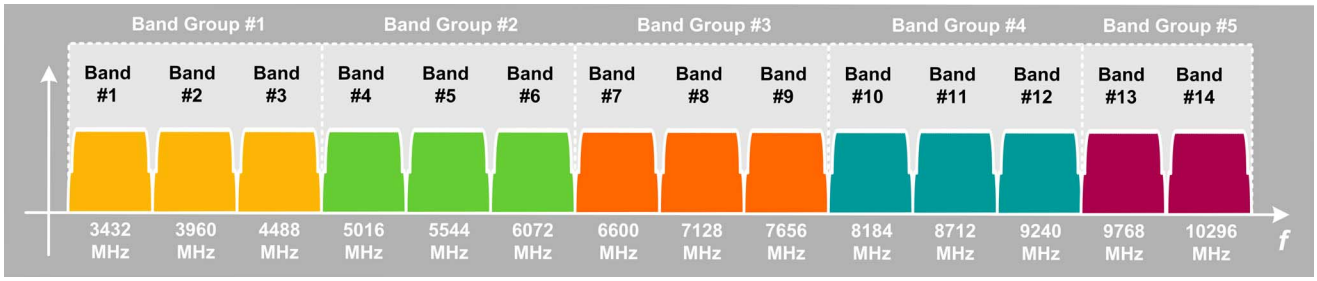

Fig. 1. Frequency plan of WiMedia Alliance for UWB.

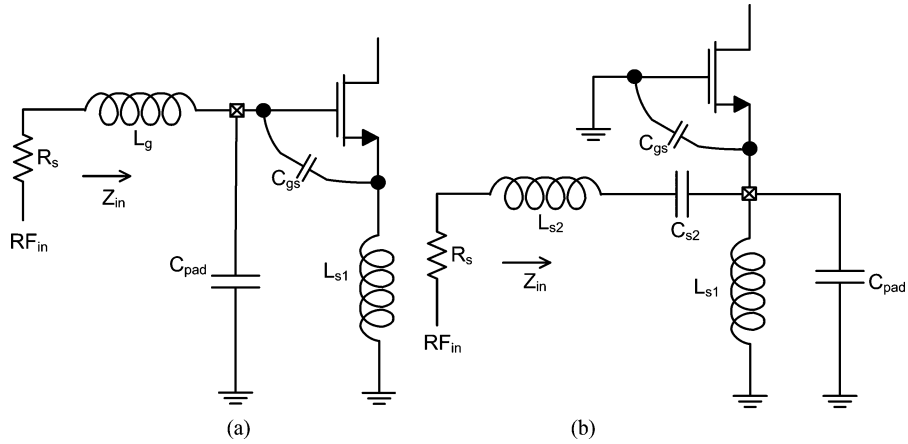

Fig. 2. (a) Common source LNA. (b) Common gate LNA.

band between 3.1 and 4.8 GHz and utilizes a CS g_m-boosting gain stage that shares the bias current with the CG amplifying stage to drastically reduce the power dissipation.

This paper is organized as follows. The basic principle of the current-reuse g_m-boosted CG configuration is explained in Section II. In the same section, the circuit topology of the proposed short-channel g_m-boosted CG LNA architecture is presented. In Section III, the small signal model and noise analysis of the proposed architecture is explained. Sections IV and V provide the circuit design and simulation and the experimental results of the proposed optimized UWB LNA, respectively. Finally, conclusions are drawn in Section VI, based on the performance of the proposed LNA. With regard to the notations in this paper, mathematical entity in the frequency domain are represented by capital letters [e.g., $Z(\omega)$] and the inverse Fourier transforms of these entities in the time domain are represented by the corresponding lower case letters [e.g., $z(t)$]. Sometimes, if it is not necessary to be mentioned, the terms ω and t are understood to be present.

II. Current-Reuse g_m-Boosted CG UWB LNA

A. Current-Reuse Technique

In literature, several narrowband and broadband current-reuse architectures have been proposed and majority of them are based on a cascade of CS stages (CS-CS) sharing the bias current [22]–[28]. To adequately isolate the cascading stages, a single inductor is used. For better isolation, in [23], LC T-network is used to provide third order isolation in the operating band along with improved noise performance. In [29], a narrowband g_m-boosted CG LNA with current reuse technique is introduced that uses a CS amplifier as the cascaded stage (CG-CS) to boost the gain. In this design, the g_m-boosting gain is provided using the transformer coils connected across the source and the gate terminals of the input device. Despite the transformer being a passive device consuming no electrical power, it is not suitable for adoption in UWB applications due to process nonlinearities and the presence of low parasitic resistance that can cause pronounced noise at the output of the amplifier. A g_m-boosted CG UWB LNA is designed in [32], which utilizes an active pMOS CS device to provide the inverting g_m-boosting gain. This design does not utilize the current-reuse technique and the bias currents through the CG amplifying stage and the CS g_m-boosting stage are not shared. In addition, it also utilizes another CS stage in cascade which is separately biased as well and causes more power dissipation. The UWB LNA circuit, proposed in this paper, takes advantage of the current-reuse technique by "stacking" the active pMOS stage (that provides the inverting g_m-boosting gain between the source and the gate terminals of the input CG stage) on top of the input CG stage ("piggy-back g_m-boosting"). Thus the new approach proposed here, is to reduce the power dissipation associated with the g_m-boosting, by implementing the "current-reused g_m-boosting", where the bias current is shared between the g_m-boosting (CS) stage and the amplifier (CG) stage. An appropriate isolation circuit is designed to separate out the CG and the CS stages at in-band AC-frequencies and for sharing the DC bias current. The isolation circuit also provides the loading at the drain terminals of the CG and the CS stages for adequate gain.

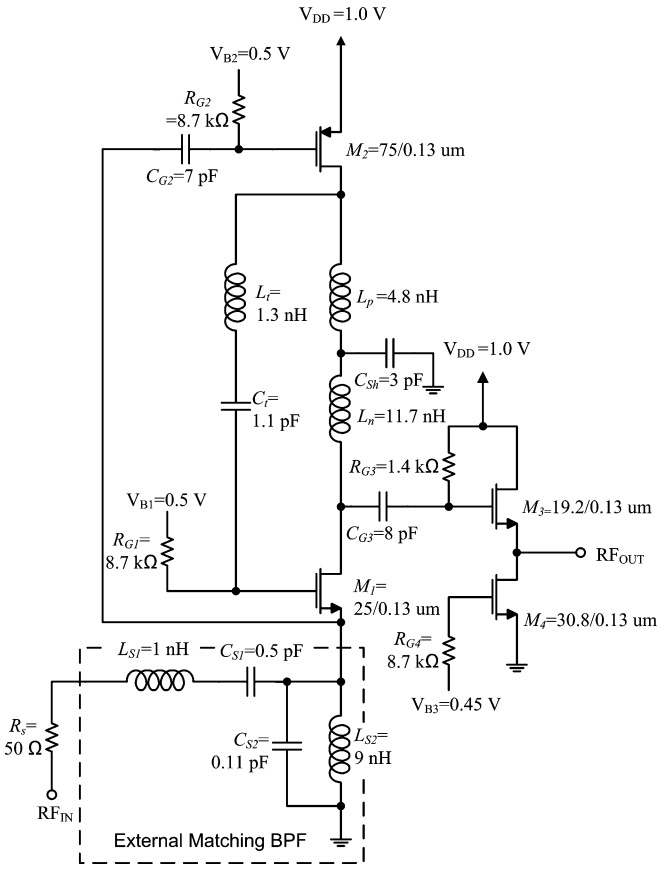

Fig. 3. Schematic of the proposed g_m-boosted current-reuse CG LNA operating in the UWB band group#1.

B. Circuit Topology

The circuit topology of the proposed UWB LNA is shown in Fig. 3. A CG amplifying device M_1 is used at the input. The CG stage with low input impedance characteristic and broadband behavior, provides NF that is almost independent of the frequency of operation. The CG stage also eliminates the Miller effect and hence provides better isolation from the output return signal. To decouple the NF from the input matching condition and to reduce the noise floor, the pMOS CS stage M_2 is used as the g_m-boosting inverting amplifier. The CS stage M_2, in conjunction with the low impedance path of the series resonant LC tank with inductor L_t and capacitor C_t, provides the inverting gain $A(\omega)$ between the source and the gate terminals of M_1. The gain $A(\omega)$ boosts the g_m of M_1 by a factor of $[1+A(\omega)]$, without having to increase its device size or the bias current [35]. As a result, better UWB noise performance and input matching is accomplished without increasing power dissipation. While the series resonant L_t and C_t provides a low impedance path between the drain of M_2 and the gate of M_1, the isolation circuit has an impedance which is adequately large to provide a high impedance path between the drains of the two MOS devices and to provide loading for reasonable gain for the g_m-boosting and the amplification stages. Since the second order resonant circuit composed of L_t and C_t presents a narrowband characteristic, it is tuned at a frequency that is nearer to the upper end of the desired band [26] instead of a mid-band frequency. In this way, the increasing impedance of this tank circuit, as the signal frequency deviates from the resonant frequency at the lower end of the desired band, is compensated by the higher intrinsic gain of the devices at lower frequencies. An LC T-network is chosen as the isolation circuit between the amplifying and the g_m-boosting stages considering its advantages over the simple single inductor circuits [23]. The third order low pass LC T-network with series inductor coils L_n and L_p and a large shunt capacitor C_{sh}, provides adequate isolation between the drain terminals of M_1 and M_2, in the frequency band of operation which is necessary for the amplification. L_n and L_p also carry the common dc bias current through M_1 and M_2 making the current-reuse possible and thus reducing the power consumption. In addition, the large capacitor C_{sh} acts as a bypass capacitor for ac-frequencies with the inductors acting as loads for the corresponding MOS devices. In order to achieve wideband input match, an off-chip fourth-order LC band-pass filter (BPF) is used at the amplifier input. The BPF starts with a series branch and ends with a shunt branch, where L_{s1} and L_{s2} are the series and shunt branch inductors, respectively. C_{s1} and C_{s2} are the corresponding series and shunt capacitors. This filter architecture is chosen in order to provide sharp out-of-band roll-off and to absorb the CG stage parasitics into the filter. The shunt branch inductor L_{s1} also facilitates the dc biasing by sinking the common drain current of M_1 (and M_2) to the circuit ground. The impedance-matched band-pass LC section is obtained using *automatic filter generation software* [33]. The devices M_3 and M_4 constitute an output buffer to provide 50 Ω match for testing purpose. The capacitors C_{G2} and C_{G3} are ac-coupling capacitors while R_{G1}, R_{G2}, R_{G3}, and R_{G4}, are biasing resistances. The bias voltages to setup the dc operating point of the amplifier are generated by on-chip current mirror circuits which are not shown in the schematic diagram of Fig. 3.

III. LNA Architectural Analysis and Design Methodology

Fig. 4 represents the equivalent small signal model of the proposed g_m-boosted current-reuse CG UWB LNA excluding the output buffer. For simplicity of the analysis, the large bypass and ac-coupling capacitors are replaced by short circuits in the small signal model. The UWB small signal input source $v_{\text{in}}(t)$, with source resistance R_s, is assumed to have constant power within the passband $[|\omega|\varepsilon(\omega_L, \omega_H)]$ and zero outside it. Hence, the BPF at the input of the amplifier is acting as a lossless matched filter within the UWB passband. It is assumed that the BPF is not inducing any noise into the circuit; hence, it is replaced by a short circuit path in the model. Similarly, the LC tank circuit composed of L_t and C_t is also replaced by a short circuit. It is also noted that in the analysis of the UWB LNA, body effect of the MOS devices M_1 and M_2 is ignored for ease of understanding. C_{gs1} and C_{gs2} are the gate-to-source capacitances of M_1 and M_2, respectively, while, v_{gs1} and v_{gs2} are the gate-to-source small signal voltages of the respective MOS devices. Although C_{gs2} is shown in the small signal model for clarity, it can be open-circuited by absorbing its susceptance, $B_2(\omega) = \omega C_{gs2}$, into the shunt branch of the BPF. g_{m1} and g_{m2} are the transconductances of M_1 and M_2 respectively. In order to study the effect of the finite short channel resistance

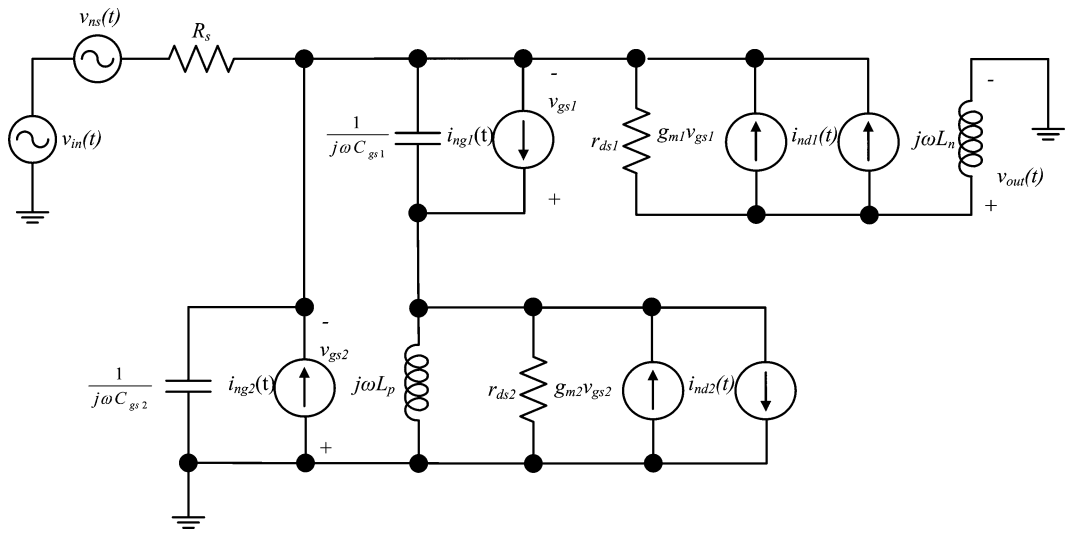

Fig. 4. Small signal equivalent representation of the proposed UWB LNA with relevant noise sources.

(due to the nanometric shrinking of the MOS devices) on the performance of the proposed UWB LNA, the short channel resistances, r_{ds1} and r_{ds2} of the corresponding MOS devices are also included in the model for analysis.

In today's nanometric processes short channel devices posses very small gate-to-source capacitance (of the order of fF) and small channel resistance. Looking at the small signal model of the LNA, it is clear that for in-band frequencies, the impedance looking into the gate of M_1, i.e., $1/j\omega C_{gs1}$ in series with R_S, is quite large and it is in parallel with $(r_{ds2}\|jX_p(\omega))$, where $X_p(\omega) = \omega L_p$. Hence, the g_m-boosting gain $A(\omega)$ provided by M_2, when the impedance looking into its drain terminal is dominated by $(r_{ds2}\|jX_p)$, can be approximated by

$$A(\omega) \approx -g_{m2}\left\{r_{ds2}\|jX_p(\omega)\right\}. \tag{1}$$

With reactance $X_n(\omega) = \omega L_n$, the overall gain $A_O(\omega)$ of the proposed CG UWB LNA is then given by equation (2), shown at the bottom of the page. In Fig. 4, $i_{nd1}(t)$ and $i_{nd2}(t)$ are the drain current noise sources of the devices M_1 and M_2, respectively, and $i_{ng1}(t)$ and $i_{ng2}(t)$ are the corresponding gate current noise sources, while, $v_{ns}(t)$ is the noise generator for the source resistance R_s. A comprehensive analysis of different types of noise in MOS devices and definitions of different noise parameters can be found in [34].

A. Noise Analysis of UWB LNA

Having established the form of the UWB LNA small signal model, the noise analysis is presented in this subsection as a design guide. If the noise power spectral density (PSD) due to $v_{ns}(t)$ is represented as $S_{v_{ns}}$, the noise factor F is then given by

$$F = 1 + \frac{S_{v_{irn1}} + S_{v_{irn2}}}{S_{v_{ns}}}. \tag{3}$$

In (3), $S_{v_{irn1}}$ and $S_{v_{irn2}}$ are the input-referred noise PSDs due to the internal noise sources of M_1 and M_2, respectively. Now, by inspecting Fig. 4, it can be proven mathematically, that a simple expression for the input referred noise voltage power spectral density (PSD) due to the internal noise sources of the device M_1, is given by

$$S_{v_{irn1}} = S_{i_{nd1}}\left[\frac{r_{ds1}^2}{\left\{1+(1+A)\,g_{m1}r_{ds1}\right\}^2}\right] \times\left\{1+R_s^2\left(B_1+B_{c1}\right)^2\right\} + S_{i_{ng1,u}}R_s^2 \tag{4}$$

where $S_{i_{nd1}}$ is the PSD of M_1's internal noise source $i_{nd1}(t)$ and $S_{i_{ng1,u}}$ is the PSD of the orthogonal component of $i_{ng1}(t)$ to $i_{nd1}(t)$ [34]. Also, $B_1(\omega)$ is the effective susceptance looking into the source of M_1 towards the ground, given by $B_1(\omega) = [1 + A(\omega)]\omega C_{gs1}$. In addition, $B_{c1}(\omega)$ is the correlation admittance which accounts for the effect of correlation between the two internal noise sources of the device M_1. After some simple derivations $B_{c1}(\omega)$ for the CG stage in (4) is found to be given by

$$B_{c1}(\omega) = \frac{B_1(\omega)}{(1+A)}\left\{\frac{1+(1+A)\,g_{m1}r_{ds1}}{r_{ds1}g_{d01}}\,|c|\sqrt{\frac{\delta}{5\gamma}}\right\}. \tag{5}$$

In (5), the correlation coefficient c, the constants γ and δ and M_1's zero-bias channel conductance g_{d01} are technology and

$$A_o(\omega) = \frac{\left\{1+(1+A)\,g_{m1}r_{ds1}\right\}.jX_n}{(R_s)\left\{1+(1+A)\,g_{m1}r_{ds1}+jB_1\left(r_{ds1}+jX_n\right)\right\}+\left(r_{ds1}+jX_n\right)} \tag{2}$$

bias dependent parameters [34]. Calculation of the input referred noise PSD $S_{v_{irn2}}$, due to the internal noise sources of the device M_2, as shown in Fig. 4, is carried out by dividing $i_{ng2}(t)$ into two orthogonal components: $i_{ng2,u}(t)$ (with PSD $S_{i_{ng2,u}}$) which is completely uncorrelated with $i_{nd2}(t)$ and $i_{ng2,c}(t)$ (with PSD $S_{i_{ng2,c}}$) which is fully correlated with $i_{nd2}(t)$ and in phase (with PSD $S_{i_{ng2}}$) [34]. The input-referred noise PSD due to all the noise sources of M_2 can then be derived to be given by (6), shown at the bottom of the page. In this composite PSD expression, the first term is contributed by the drain current noise of M_2, the second term by the correlated part of the induced gate current noise, the third term arises from the cross-correlation of these two noise sources and the final term is the contribution of the uncorrelated induced gate current noise of M_2. Inspecting (3) and (4), it is evident that the g_m-boosting by the factor $(1 + A)$ can increase the system signal-to-noise ratio (SNR) considerably. In addition, it can be seen from (4) that with the matched BPF network at the input of the LNA, the SNR can be further increased by setting $B_1(\omega) = -B_{c1}(\omega)$. In general, for noise optimization, the overall susceptance looking at the source of M_1, $B_{\text{in,opt}}(\omega) = -B_{c1}(\omega)$. This can be achieved by setting the reactive components of the BPF in conjunction with the size of $B_1(\omega)$, so that over all the value of $B_{\text{in,opt}}(\omega)$ is achieved. The effect of the short-channel resistance can also be appreciated by analyzing (4). Reducing r_{ds1} can reduce the channel current noise without bound and theoretically at zero channel resistance, the channel current noise completely disappears. However, practically, this is not feasible as r_{ds} cannot be technologically controlled to such a limiting value. From (6), it is apparent that increasing the g_m-boosting gain $A(\omega)$ can increase the noise PSD due to M_2, resulting in a reduction of the system SNR, which is highly undesirable. On the other hand, it can be appreciated that the noise contribution by M_2 can be minimized by keeping high device transconductance, g_{m2}, as it appears in the denominator of two noise terms. However, an increase in g_{m2} would also increase the g_m-boosting gain $A(\omega)$ that can degrade the SNR due to M_2's noise sources. As a compromise, $A(\omega)$ can be kept within an acceptable limit by maintaining low effective load $(r_{ds2}||jX_p)$ at the drain terminal of M_2 while still designing for higher g_{m2}. The total noise factor of the proposed g_m-boosted UWB CG LNA is then computed by substituting (4) and (6) into (3) and solving for F, which is then given by

$$F = \frac{\gamma g_{d01}}{R_s}\left[\frac{r_{ds1}^2}{\{1+(1+A)\,g_{m1}r_{ds1}\}^2}\right] \times \left\{1+R_s^2\,(B_1+B_{c1})^2\right\} + \frac{\delta B_1^2 R_s}{5g_{d01}} + \frac{\gamma g_{d02}}{R_s}\beta^2 + \frac{\delta B_2^2 R_s}{5g_{d02}} + 2\beta B_2\sqrt{\frac{\delta\gamma}{5}} \tag{7}$$

where $\beta(\omega)$ is a frequency dependent parameter of the dimension Ω (ohms) and is given by (8), shown at the bottom of the page. In addition, γ and δ are assumed to be the same for M_1 and M_2 , while g_{d01} and g_{d02} are zero-bias channel conductances for M_1 and M_2, respectively [34].

B. Input Matching and Noise

In the previous subsection, detailed noise analysis of the proposed UWB LNA was carried out. From (7) and (8) it can be seen that the g_m-boosting gain $A(\omega)$ has an inverse relationship with the input referred noise due to M_1 and on the other hand, a direct relationship with the input referred noise due to M_2. It is now necessary to observe the effect of the short channel finite resistance and the g_m-boosting gain $A(\omega)$ on the input matching characteristics of the proposed UWB LNA. Revisiting the small signal model of the LNA in Fig. 4, the frequency domain representation of the input admittance of the proposed circuit, as seen by the UWB source, is given by

$$Y_{\text{in}}(\omega) = \frac{1+\{1+A(\omega)\}\,g_{m1}r_{ds1}}{r_{ds1}+jX_n(\omega)} + jB_1(\omega) + jB_2(\omega). \tag{9}$$

If $B_1(\omega)$ and $B_2(\omega)$ are relatively small and absorbed by the $L_{s2} - C_{s2}$ shunt branch of the BPF at the source terminal of M_1, the admittance can be separated into its real and imaginary parts that are given by

$$Y_{\text{in}}(\omega) = \frac{\{1+(1+A)\,g_{m1}r_{ds1}\}.r_{ds1}}{r_{ds1}^2+X_n^2} - j\frac{\{1+(1+A)\,g_{m1}r_{ds1}\}.X_n}{r_{ds1}^2+X_n^2}. \tag{10}$$

$$S_{v_{irn2}} = S_{i_{nd2}}\frac{[\{1+(1+A)\,g_{m1}r_{ds1}\}R_s + r_{ds1} - B_1R_sX_n]^2 + (X_n + B_1R_sr_{ds1})^2}{g_{m2}^2\,(r_{ds1}^2+X_n^2)} + S_{i_{ng2,c}}R_s^2 + 2\sqrt{S_{i_{ng2,c}}S_{i_{nd2}}R_s^2\frac{[\{1+(1+A)\,g_{m1}r_{ds1}\}R_s + r_{ds1} - B_1R_sX_n]^2 + (X_n + B_1R_sr_{ds1})^2}{g_{m2}^2\,(r_{ds1}^2+X_n^2)}} + S_{i_{ng2,u}}R_s^2 \tag{6}$$

$$\beta(\omega) = \frac{1}{g_{m2}}\sqrt{\frac{[\{1+(1+A)\,g_{m1}r_{ds1}\}R_s + r_{ds1} - B_1R_sX_n]^2 + (X_n + B_1R_sr_{ds1})^2}{(r_{ds1}^2+X_n^2)}} \tag{8}$$

The effect of the g_m-boosting can be appreciated from (10), where g_{m1} is increased by a factor $\{1 + A(\omega)\}$ resulting in higher effective transconductance of M_1 and better input matching without the expense of more power supply drain. $Y_{\text{in}}(\omega)$ reduces to $(1 + A)g_{m1}$ when long channel assumption is made $(r_{ds1} \rightarrow \infty)$ which is the published input admittance of long-channel g_m-boosted CG LNA [15]. It is clear from (10) that the imaginary part of $Y_{\text{in}}(\omega)$ represents a grounded inductor in parallel with the shunt branch of the BPF and can be absorbed into it. Due to the short-channel (finite r_{ds1}), the effect of the load at the drain of M_1 also appears at its source and causes a reduction in the input admittance of the CG stage (which is not desirable). It indicates a tradeoff between the gain of the LNA, its input matching and the power consumption. This is because, for higher gain a larger $X_n(\omega)$ would be required, which would force setting a higher value for g_{m1} (higher power dissipation) in order to bound the real part of $Y_{\text{in}}(\omega)$ for impedance matching to 50 Ω. Hence, the effective transcoductance of the short-channel CG stage should be set higher than 20 ms for better input match.

As a concluding remark with regard to design methodology, the g_m-boosting gain $A(\omega)$ must be set carefully so that the reduction in the drain current noise due to M_1 is not offset by the deterioration of the input referred noise due to M_2 [comparing (4) and (6)]. As discussed in the previous subsection, g_{m2} can be increased while maintaining low effective load at the drain of M_2, so as to keep the input referred noise component due to M_2 in the overall SNR to a minimum.

IV. UWB LNA Circuit Design and Simulation

The design of the proposed CMOS UWB LNA, as shown in Fig. 3, is based on the IBM 130-nm RFCMOS process. For better performance at high frequencies and lower parasitics, a minimum channel length of 130 nm is chosen for all the transistors in the circuit. The extensive circuit simulations, optimization and chip layout of the proposed design was carried out using *Cadence* tools. Following the analysis and the design methodology in Section III, g_{m1} and g_{m2} are set at 11.5 and 10.5 ms, respectively. For these transconductance values, the widths of M_1 and M_2 are set at 25 and 75 μm respectively, that requires a reused bias current of around 1.25 mA. The resulting approximate unity gain frequencies of $f_{T1} = 180$ GHz (for M_1) and $f_{T2} = 55$ GHz (for M_2) are more than five times the maximum frequency of the operating band and hence provides sufficient intrinsic bandwidth for achieving the specified performance of the UWB LNA. After iterative simulations, keeping in view the tradeoffs explained in the previous section, L_n and L_p are designed as 11.7 and 4.8 nH inductors, respectively, to provide adequate UWB gain and noise performance. L_p in conjunction with g_{m2} provides a gain magnitude ($|A(\omega)|$) of around 1.33 (peak) at 4.2 GHz, which is chosen to be within the upper-half of the operating band through rigorous simulations in order to optimize the noise within the band. This makes the effective transconductance of M_1 around 27 mS at this frequency. The effective transconductance is set higher than 20 mS to take into account the effect of the short channel finite resistance as per (10). As mentioned earlier, the UWB LNA gain and noise is optimized at a frequency, nearer to the upper cutoff frequency of the operating band with the realization that, at lower frequencies these can be compensated by the higher intrinsic gain of the devices. For the same reason, the resonant frequency of the $L_t - C_t$ tank is chosen as 4.2 GHz using a 1.3 nH inductor and a 1.1 pF capacitor. For low power consumption, the dc supply voltage is kept at 1.0 V and the gate terminals of M_1 and M_2 are biased at 500 mV with the drain to source voltage drops for each of the MOS devices set at 500 mV. The gate-bias voltages are generated by current mirror circuits so as to minimize power consumption. The source-follower devices were sized appropriately ($M_3 = 19.2$ μm and $M_4 = 30.8$ μm) to provide 50 Ω output match. The external BPF components are chosen considering the presence and the absorption of the front-end (pad, bonding wire and package) parasitic reactances including the inductive susceptance of the UWB LNA's input admittance, in order to provide better broadband input match with sharp out-of-band signal rejection. For effective BPF design, the *Cadence Spectre-RF* simulator is used to extract device operating parameters for both M_1 and M_2. The important extracted parameters were: $C_{gs1} = 9.5$ fF, $C_{gs2} = 30.1$ fF, $r_{ds1} = 932$ Ω and $r_{ds2} = 1250$ Ω. Fig. 5 shows the composite circuit topology of the RF signal input interconnect path showing a cascaded network of the input impedance of the UWB LNA, wire-bond, package parasitics and the external band-pass filter. Here, $R_{\text{in}}(\omega)$ and $L_{\text{in}}(\omega)$ are the equivalent resistance and inductance at the source terminal of M_1 and can be computed using (10). $C_{\text{in}}(\omega)$ is the equivalent capacitance at the source terminal of M_1 and is a parallel combination of $B_1(\omega)$, $B_2(\omega)$ and the bonding-pad capacitance ($C_{\text{pad}} \approx 0.2$ pF). Here, as a tradeoff the effective admittance at the input of the LNA is absorbed in the input matching network *(power match)* instead of matching with the correlation admittance as per discussion on noise optimization in Section III-A *(noise match)*, which is compensated by the g_m-boosted lowering of the overall noise figure. The overall input impedance of the amplifier in the operating band is plotted using the smith-chart as shown in Fig. 6. The smith chart trace depicts the variation of the impedance looking into the RF signal input interconnect path, indicating a close match with 50 Ω source resistance at 4.1 GHz and the amount of mismatch (radial distance from the origin to a point on the trace) at the other frequencies within the pass-band between the corner frequencies (3.1 and 4.8 GHz, respectively, at the bottom and top terminus of the trace).

V. Fabrication and Experimental Results

The UWB LNA was fabricated using the IBM 130-nm RFCMOS process. The photomicrograph of the fabricated die is shown in Fig. 7 with chip area of 640 μm $\times$ 470 μm (0.301 sq. mm) including the bonding pads. All the on-chip active devices are fabricated with fingered gate terminals to reduce the gate-resistance so that the intrinsic f_T of the devices are maximized and their gate-resistance noise PSDs are minimized. All the on-chip inductors were fabricated as octagonal spirals with central cavity (for high Q) using 5 μm wide traces of top thick aluminum layer MA with copper layer E1 as underpass contact to the spiral center. The outer diameters of the on-chip inductors are, respectively, 250, 180, and 100 μm for L_n, L_p, and L_t. The shunt capacitor C_{sh}, the bypass capacitors C_{G2}

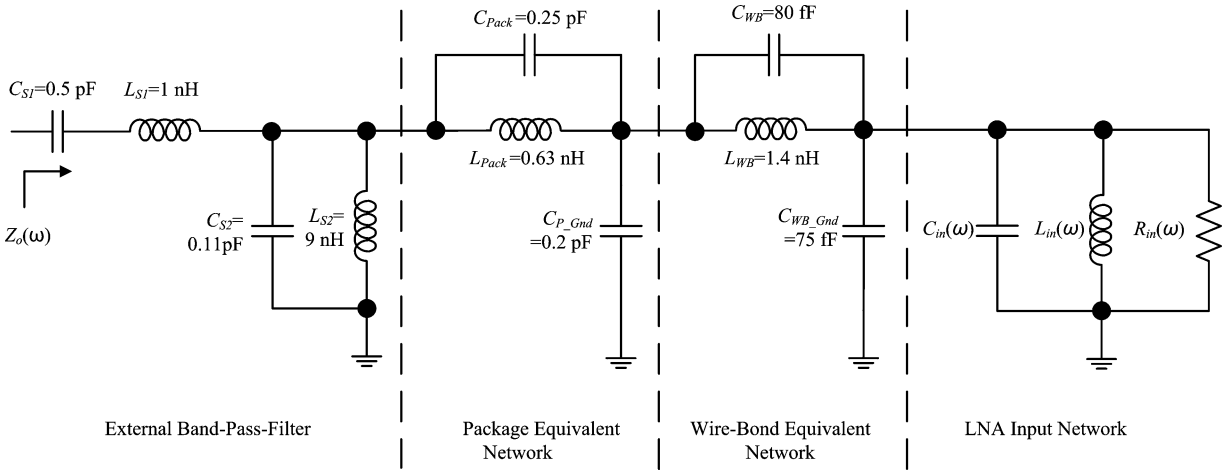

Fig. 5. Composite circuit topology of the RF signal input interconnect path showing a cascaded network of the input impedance of the UWB LNA, wire-bond, package, and the external band-pass filter.

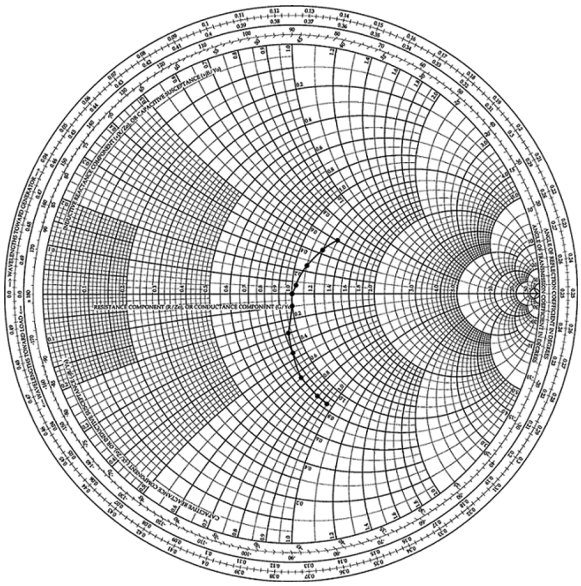

Fig. 6. Smith-chart trace depicting the variation of the impedance looking into the RF signal input interconnect path, indicating a match with 50 Ω source resistance at 4.1 GHz and the amount of mismatch (radial distance from the origin to the trace) at the corner frequencies (3.1 and 4.8 GHz, respectively, at the bottom and top terminus of the trace).

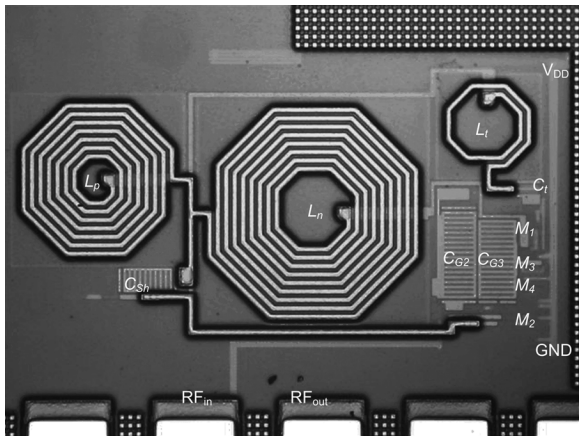

Fig. 7. Microphotograph of the proposed LNA with labels showing all the active and passive components.

and C_{G3}, and the series tank capacitor C_t are fabricated as MIM capacitors using the thin metal layers QY and HY with thin dielectric aluminum nitride sandwiches, interconnected with the enclosing layers E1 and LY. All the resistors providing dc biasing and the current mirror and ac blocking terminations are fabricated using the high sheet resistance shallow p^+ poly layer. All the active and passive components are labeled on the chip photo. Transient and AC measurements were carried out using the Agilent DCA J 86100C and Agilent E4428C ESG signal generator. Network-level characterization was carried out by power wave measurements in the TDR/TDT mode [40]. All measurements include trace and connector losses. Fig. 8 shows the simulated and measured input reflection coefficient S_{11}. In the simulation phase, S_{11} is kept in the range $< -$ 10 dB. The degradation in the measured result is mainly due to the presence of the CG input susceptances, bonding-pad parasitics, bonding wire, packaging traces, and the inaccuracies in the external BPF components. Despite these intervening terminations causing signal reflection, the S_{11} is below $-$ 8 dB over the entire frequency band of operation which indicates reasonably acceptable input matching. The S_{11} plot is also found to be roughly close to its theoretical estimate in the smith chart of Fig. 6. Fig. 9 shows the forward power-gain curve and its comparison with the simulation. The forward-gain S_{21} is measured to be around 13 dB with the dc power consumption of around 3.4 mW (which includes the power dissipation and the 6 dB gain loss at the source-follower output buffer). The gain is almost flat with some degradation at the upper UWB frequencies. This gain erosion is mainly due to the increase in the substrate leakage at higher frequencies. Fig. 10 presents the achieved noise figure for the proposed LNA. The measured noise figure of the LNA is below 4.5 dB in the pass-band with a $\mathrm{NF}_{\min}$ of around 3.5 dB which is acceptable for an UWB LNA [13], [37]. This noise performance is achieved in power match condition and can be further optimized (reduced) by designing the circuit elements at the source input of M_1 for noise match (setting $B_{\mathrm{in,opt}}(\omega) = -B_{c1}(\omega)$), as per discussion

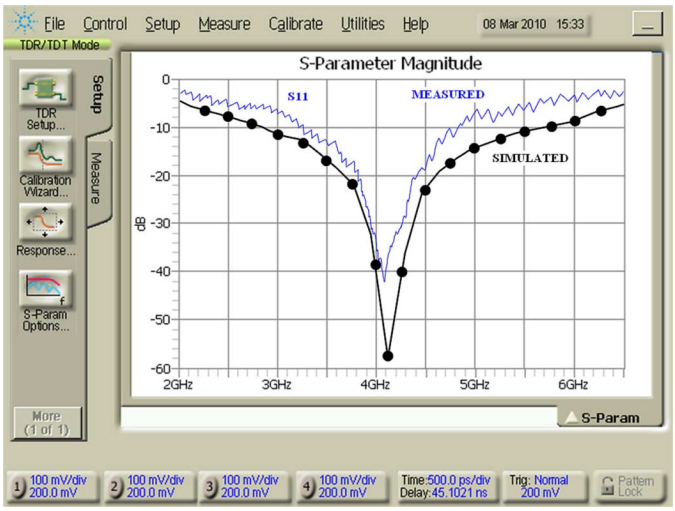

Fig. 8. Input reflection coefficient (S_{11}).

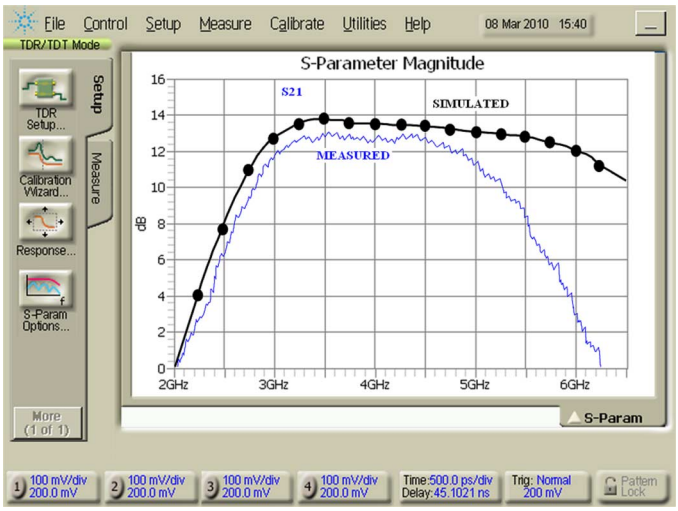

Fig. 9. Forward gain (S_{21}).

on noise optimization in Section III-A. The g_m-boosting CS stage noise contribution can also be optimized by employing inductive source degeneration to M_2. Using this technique, input matching characteristics of the LNA can be further enhanced, as the inductive degenerated CS stage would contribute a resistive component parallel to the input impedance of the CG LNA given by (10). Figs. 11 and 12 show the remaining measured S-parameters and their comparison with the simulation. The LNA provides very good reverse isolation as the use of the CG topology removes the Miller effect. Hence, the measured S_{12} is less than -40 dB within the pass-band. The reverse isolation deteriorates at higher frequencies due to increased parasitic feed back at higher frequencies. The measured S_{12} is higher than the simulated value due to the effect of the additional stray feedback paths not accounted for by the parasitic extraction simulator. The measured output matching coefficient S_{22} is less than -14 dB throughout the operating band and is almost constant largely due to the broadband behavior of the output impedance of the output source-follower buffer. In order to determine the spurious free dynamic range ceiling, the IIP3

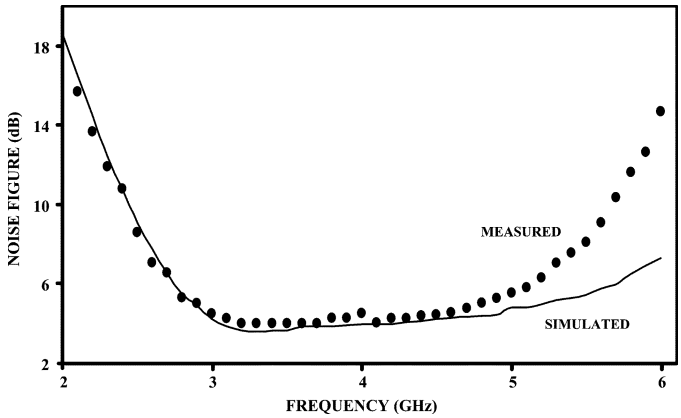

Fig. 10. Noise figure (NF).

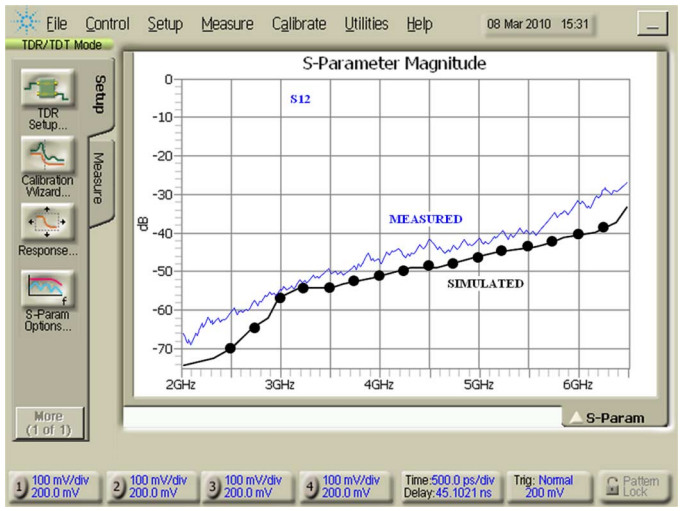

Fig. 11. Reverse isolation (S_{12}).

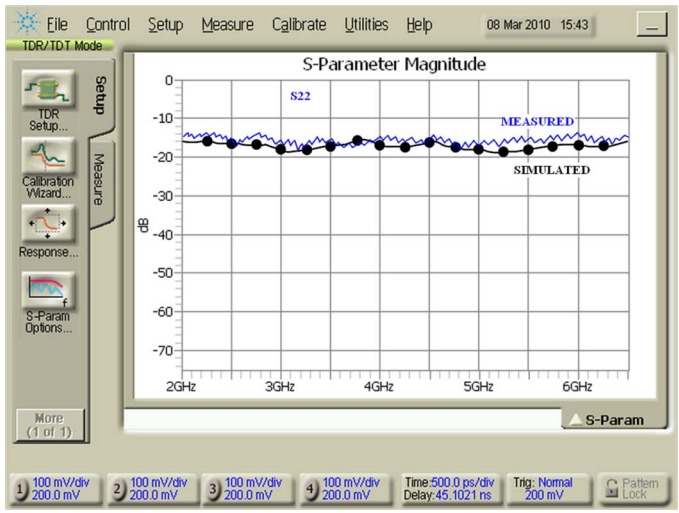

Fig. 12. Output reflection coefficient (S_{22}).

and the 1-dB compression point were evaluated. Accordingly, a two-tone test was carried out at the mid-band frequency of 3.9 GHz with a 500 MHz tone separation. The measurements indicate an input-referred IP3 of -6.1 dBm and an input-referred 1-dB compression point ($\mathrm{ICP}_{1\,\mathrm{dB}}$) of -15.4 dBm, as

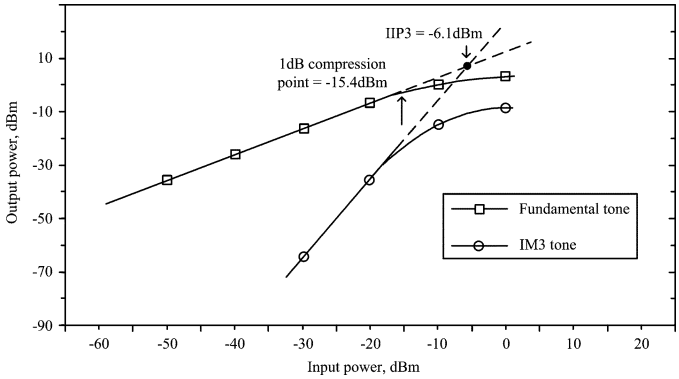

Fig. 13. IIP3 and the 1 dB compression point for the UWB LNA at 3.9 GHz.

TABLE I
SUMMARY OF THE g_m-BOOSTED CG UWB LNA PERFORMANCE AND COMPARISON WITH PREVIOUS RECENTLY PUBLISHED DESIGNS

	This work	[40]	[41]	[17]#%	[39]	[38]*%
Technology (nm)	130	180	180	45	180	130
Year	2010	2010	2010	2009	2008	2006
$Bandwidth_{3\text{-}dB}$ (GHz)	3.1-4.8	3.4-11	3-4.8	2.5-9.6	3.1-4.8	2-4.6
Input return loss S_{11}(dB)	<-8	<-10	<-10	<-15	<-10	<-10
Reverse isolation S_{12}(dB)	<-40	<-65	N/A	N/A	N/A	N/A
Forward gain S_{21} (dB)	13	14	15	12.5	13.9	9.5
Output return loss S_{22}(dB)	<-14	N/A	N/A	N/A	<-8.2	N/A
Minimum noise figure, NF_{min} (dB)	3.5	4.7	3.5	5.5	4.68	3.5
Power dissipation P_{diss} (mW)	3.4	30	5.0	5.3	14.6	16.5
Supply voltage (V)	1.0	2.5	1.8	1.2	1.8	1.5
Chip-area (mm^2)	0.4^	1.11	0.76	0.441	0.945	1.08
I/R compression point ICP_{1dB} (dBm)	-15.4	-14.5	-18.0	N/A	N/A	-6.0
I/R third order intercept point IIP_3 (dBm)	-6.1	-5.3	N/A	N/A	0.12	-0.8
#: Simulation only %: Differential *: CS input stage N/A: Not available						
I/R: Input referred ^: Estimated, including bonding pads and external filter						

shown in the Fig. 13. Finally, Table I summarizes the measured performance of the proposed current-reuse g_m-boosted CG UWB LNA and provides a comparison of the circuit with other recently reported designs. The improvements attained by the proposed current reuse g_m-boosted architecture is clearly evident when compared to these other UWB LNA circuits, particularly for low-voltage and low-power solution.

VI. CONCLUSION

This paper demonstrated the design of a low power LNA architecture, operating in the 3.1–4.8 GHz UWB range, designed using the IBM 130-nm CMOS process. This paper presents a new approach to boost the g_m ("piggy-back g_m-boosting") of the CG LNA by adopting a current-reuse technique to reduce the power dissipation by sharing the bias current between the g_m-boosting and the UWB signal amplifying stages. The expressions for the LNA to represent and optimize the noise factor have been derived. Various design tradeoffs between the g_m-boosting gain, input matching, gain of the amplifying stage and noise contributions by the active devices constituting the complete g_m-boosted CG UWB LNA are also explained and analyzed. Measured results show satisfactory performance of the proposed LNA with a power consumption of only 3.4 mW. This technique thus provides an avenue for achieving broadband low noise performance using the CG topology.

REFERENCES

[1] G. Weinberger, "The new millennium: Wireless technologies for a truly mobile society," in *Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2000, pp. 20–24.
[2] C. Enz, "An MOS transistor model for RF IC design valid in all regions of operation," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 1, pp. 342–359, Jan. 2002.
[3] Y. Cheng, M. J. Deen, and C. H. Chen, "MOSFET modeling for RF IC design," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1286–1303, Jul. 2005.
[4] FCC, Washington, DC, "First report and order, revision of Part 15 of the commission's rules regarding ultra wideband transmission systems," DC ET Docket 98-153, 2002.
[5] A. Batra, J. Balakrishnan, G. R. Aiello, J. R. Foerster, and A. Dabak, "Design of a multiband OFDM system for realistic UWB channel environments," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 9, pp. 2123–2138, Sep. 2004.
[6] M. M. Reja, K. Moez, and I. Filanovsky, "An area-efficient multistage 3.0- to 8.5-GHz CMOS UWB LNA using tunable active inductors," *IEEE Trans. Circuits Syst. II, Expr. Briefs*, vol. 57, no. 8, pp. 587–591, Aug. 2010.
[7] M. Battista, J. Gaubert, M. Egels, S. Bourdel, and H. Barthelemy, "High-voltage-gain CMOS LNA for 6–8.5-GHz UWB receivers," *IEEE Trans. Circuits Syst. II, Expr. Briefs*, vol. 55, no. 8, pp. 713–717, Aug. 2008.
[8] J. Gaubert, M. Egels, P. Pannier, and S. Bourdel, "Design method for broadband CMOS RF LNA," *Electron. Lett.*, vol. 41, no. 7, pp. 383–384, 2005.
[9] H. Y. Yang, Y. S. Lin, and C. C. Chen, "2.5 dB NF 3.1–10.6 GHz CMOS UWB LNA with small group-delay variation," *Electron. Lett.*, vol. 44, no. 8, pp. 528–529, 2008.
[10] C. Y. Cha and S. G. Lee, "A 5.2 GHz LNA in 0.35 μm CMOS utilizing inter-stage series resonance and optimizing the substrate resistance," in *Proc. Eur. Solid-State Circuits Conf.*, 2002, pp. 339–342.
[11] H. Zhang, X. Fan, and S. Sinencio, "A low-power, linearized, ultra-wideband LNA design technique," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 320–330, Feb. 2009.
[12] Y. Shim, C. W. Kim, J. Lee, and S. G. Lee, "Design of full band UWB common-gate LNA," *IEEE Microw. Wirel. Components Lett.*, vol. 17, no. 10, pp. 721–723, Oct. 2007.
[13] A. Bevilacqua and A. M. Niknejad, "An ultrawideband CMOS low noise amplifier for 3.1–10.6 GHz wireless receivers," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2259–2268, Dec. 2004.
[14] A. Ismail and A. A. Abidi, "A 3–10 GHz low noise amplifier with wideband LC-ladder matching network," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2269–2277, Dec. 2004.
[15] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. P. de Gyvez, D. J. Allstot, and E. Sanchez-Sinencio, "A capacitor cross-coupled common-gate low noise amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 12, pp. 875–879, Dec. 2005.
[16] WiMedia Alliance, "Multi-band OFDM physical layer specifications, PHY Version 1.2," 2007.
[17] D. Ponton, P. Palestri, D. Esseni, L. Selmi, M. Tiebout, B. Parvais, D. Siprak, and G. Knoblinger, "Design of ultra-wideband low-noise amplifiers in 45-nm CMOS technology: Comparison between planar bulk and SOI FinFET devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 5, pp. 920–932, May 2009.
[18] T. K. K. Tsang, K. Y. Lin, and M. N. E. Gamal, "Design techniques of CMOS ultra-wide-band amplifiers for multistandard communications," *IEEE Trans. Circuits Syst. II, Expr. Briefs*, vol. 55, no. 3, pp. 214–218, Mar. 2008.
[19] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 745–759, Jun. 1997.

[20] T. K. Nguyen, C. H. Kim, G. J. Ihm, M. S. Yang, and S. G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 5, pp. 1433–1442, May 2004.
[21] V. H. Le, S. K. Han, J. S. Lee, and S. G. Lee, "Current-reused ultra low power, low noise LNA+mixer," *IEEE Microw. Wirel. Component Lett.*, vol. 19, no. 11, pp. 755–757, Nov. 2009.
[22] M. D. Wei, S. F. Chang, and Y. C. Liu, "A low-power ultra-compact CMOS LNA with shunt-resonating current-reused topology," in *Proc. 3rd EMICC*, 2008, pp. 350–353.
[23] C. Y. Cha and S. G. Lee, "A 5.2-GHz LNA in 0.35 μm CMOS utilizing inter-stage series resonance and optimizing the substrate resistance," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 669–672, Apr. 2003.
[24] Z. D. Huang, Z. M. Lin, and H. C. Lai, "An high gain low noise amplifier with current-reused technique for UWB applications," in *Proc. IEEE Conf. EDSSC*, 2007, pp. 977–980.
[25] H. L. Kao, A. Chin, K. C. Chang, and S. P. McAlister, "A low-power current-reuse LNA for ultra-wideband wireless receivers from 3.1 to 10.6 GHz," in *Proc. Topical Meet. SMIC RF Syst.*, 2007, pp. 257–260.
[26] Y. J. Lin, S. S. H. Hsu, J. D. Jin, and C. Y. Chan, "A 3.1–10.6 GHz ultra-wideband CMOS low noise amplifier with current-reused technique," *IEEE Microw. Wirel. Components Lett.*, vol. 17, no. 13, pp. 232–234, Mar. 2007.
[27] R. L. Wang, S. C. Chen, C. L. Huang, C. H. Liu, and Y. S. Lin, "2–6 GHz current-reused LNA with transformer-type inductors," in *Proc. APMC*, 2008, pp. 1–4.
[28] T. Taris, Y. Deval, and J. B. Begueret, "Current reuse CMOS LNA for UWB applications," in *Proc. 34th ESSCIRC*, 2008, pp. 294–297.
[29] J. S. Walling, S. Shekhar, and D. J. Allstot, "A g_m-boosted current-reuse LNA in 0.18 μm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, 2007, pp. 613–616.
[30] L. Cai, Z. Fu, and L. Huang, "Design of common gate UWB LNA in CMOS," in *Proc. ASICON*, 2009, pp. 1201–1204.
[31] F. Lu and L. Xia, "A CMOS LNA with noise cancellation for 3.1–10.6 GHz UWB receivers using current-reuse configuration," in *Proc. 4th ICCSC*, 2008, pp. 824–827.
[32] C. Y. Wu, Y. K. Lo, and M. C. Chen, "A 3.1–10.6 GHz CMOS direct-conversion receiver for UWB applications," in *Proc. IEEE ICECS*, 2006, pp. 1328–1331.
[33] Nuhertz Technol., LLC, Phoenix, AZ, "Filter Solutions 10.0," 2005. [Online]. Available: http://www.nuhertz.com
[34] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2004.
[35] D. J. Allstot, X. Li, and S. Shekhar, "Design considerations for CMOS low-noise amplifiers," in *Proc. IEEE Radio Freq. Integr. Circuit Symp.*, 2004, pp. 97–100.
[36] D. Pepe and D. Zito, "22.7-dB gain -19.7-dBm $\mathrm{Icp}_{1\ \mathrm{dB}}$ UWB CMOS LNA," *IEEE Trans. Circuits Syst. II, Expr. Briefs*, vol. 56, no. 9, pp. 689–693, Sep. 2009.
[37] B. Razavi, T. Aytur, C. Lam, F. R. Yang, R. H. Yan, H. C. Kang, C. C. Hsu, and C. C. Lee, " Multiband UWB transceivers," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2005, pp. 141–148.
[38] A. Bevilacqua, C. Sandner, A. Gerosa, and A. Neviani, "A fully integrated differential CMOS LNA for 3–5-GHz ultrawideband wireless receivers," *IEEE Microw. Wirel. Components Lett.*, vol. 16, no. 3, pp. 134–136, Mar. 2006.
[39] M. I. Jeong, J. N. Lee, and C. S. Lee, "Design of UWB switched gain controlled LNA using 0.18 μm CMOS," *Electron. Lett.*, vol. 44, no. 7, pp. 477–478, Mar. 2008.
[40] S. M. Hasan, "Analysis and design of a multi-stage CMOS band-pass low noise pre-amplifier for ultra-wide-band RF receiver," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 4, pp. 638–651, Apr. 2010.
[41] C. P. Liang, P. Z. Rao, T. J. Huang, and S. J. Chung, "Analysis and design of two low-power ultra-wideband CMOS low-noise amplifiers with out-band rejection," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 2, pp. 277–286, Feb. 2010.
[42] J. P. Pavon, S. Shankar, V. Gaddam, K. Challapali, and C. T. Chou, "The MBOA-WiMedia specification for ultra wideband distributed networks," *IEEE Commun. Mag.*, vol. 44, no. 6, pp. 128–134, Jun. 2006.
[43] H. Zheng, S. Lou, D. Lu, C. Shen, T. Chan, and H. C. Luong, "A 3.1 GHZ-8.0 GHz single chip transceiver for MB-OFDM UWB in 0.18-μ m CMOS process," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 414–426, Feb. 2009.

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